IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	001701.00059
Yoshiaki FUKUZUMI et al.			
Serial No.:	09/783,023	Group Art Unit:	2823
Filed:	February 15, 2001	Examiner:	G. Fourson, III
For:	SEMICONDUCTOR DEVICE USING FUSE/ANTI-FUSE SYSTEM AND METHOD OF MANUFACTURING THE SAME	Confirmation No.:	6061

APPEAL BRIEF

Mail Stop: Appeal Brief-Patents
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief in accordance with 37 C.F.R. § 1.192, filed in triplicate in support of appellants' October 14, 2003 Notice of Appeal. Appeal is taken from the Final Office Action mailed June 11, 2003, and the Advisory Action mailed October 10, 2003. Please charge any necessary fees in connection with this Appeal Brief to our Deposit Account No. 19-0733.

REAL PARTY IN INTEREST

The owner of this application, and the real party in interest, is Kabushiki Kaisha Toshiba.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

STATUS OF CLAIMS

Claims 1-11 are rejected, claims 12-20 are canceled, and claim 21-31 are withdrawn. Only pending claims 1-11 are shown in the attached appendix.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of U.S. patent no. 5,629,227 to Chen, U.S. patent no. 6,130,469 to Bracchitta et al. ("Bracchitta"), and Wolf, S., "Silicon Processing of the VLSI Era," Vol. 2 Process Integration ("Wolf").

Appellants hereby appeal the rejection of claims 1-11.

STATUS OF AMENDMENTS

The Amendment After Final Rejection responsive to the final Office Action of June 11, 2003, filed August 21, 2003, has been entered and all prior amendments have been entered. Appellants are concurrently submitting an Amendment After Final to correct an obvious antecedent basis problem in claim 9 and an obvious error in the specification. Specifically, "portions" has been amended to read --portion-- in claim 9 and "FIGS. 22 to 28" has been replaced with --FIGS. 28 to 33--. Entry of these amendments are respectfully requested. Claim 9 as presented in the attached appendix assumes entry of the Amendment After Final filed herewith.

SUMMARY OF INVENTION

In making reference herein to various portions of the specification and drawings in order to explain the claimed invention (as required by 37 C.F.R. § 1.192(c)(5)), Appellants do not

intend to limit the claims; all references to the specification and drawings are illustrative unless otherwise explicitly stated.

The present invention is directed to a semiconductor device that facilitates the formation of a gate insulating film having a desired breakdown voltage in a fuse/antifuse system. Specification, p. 6, ll. 13-21.

Referring to Fig. 1, formed in a silicon substrate 11 are first concave portion 12 forming an element isolation region, a second concave portion 13 forming an aligning mark portion, and a concave portion 14 for an antifuse portion. Specification, p. 17, ll. 5-14. As is apparent from inspection of Fig. 1, concave portion 14 (corresponding to the second concave portion recited in claim 1) has a depth from a top surface of the semiconductor substrate 11, substantially equal to a depth of the first concave portion 12 (corresponding to the first concave portion recited in Fig. 1). An element isolating region 16 of STI structure is formed in the first concave portion 12 with silicon oxide film 15 formed in the first concave portion 12. Specification, p. 17, ll. 15-23; Fig. 2.

A gate insulating film 18 is formed on the entire surface of the substrate, followed by formation of a polysilicon film 19 on the gate insulating film 18 and formation of a tungsten film 20 on the polysilicon film 19. Specification, p. 18, ll. 6-14; Fig. 4. Subsequently, the gate insulating film 18, polysilicon film 19, and tungsten film 20 are selectively removed resulting in gate electrode 22 including gate insulating film 18a (corresponding to the first gate insulating film recited in claim 1), polysilicon film 19 (corresponding to the first conductive film recited in claim 1) and tungsten film 20, and gate electrode 24 for an anti-fuse portion formed in a bottom surface of the concave portion 14 including gate insulating film 18b (corresponding to the second gate insulating film), polysilicon film 19 and tungsten film 20 (corresponding to the second

conductive film recited in claim 1). Specification, p. 18, l. 15 to p. 19, l. 1; Fig. 5. Thereafter, following an additional step(s), the structure in Fig. 6 results. Due to damage done to the bottom surface of the concave portion 14 in forming the concave portions 12, 13 and 14, the breakdown voltage of the gate insulating film 18b formed in the concave portion 14 can be lowered as compared to the gate insulating film 18a of the transistor formed on the substrate surface. Specification, p. 19, ll. 19-26.

Figs. 8-10 show illustrative implementations of the claim 2 invention where the second gate insulating film and the second conductive film are formed on the bottom surface of the second concave portion, on at least one side surface of the second concave portion and on the semiconductor substrate, and a top surface of the first conductive film is flush with a surface of the second conductive film formed on the semiconductor substrate. Also, Figs. 8-10 show illustrative implementations of the claim 3 invention, where the second gate insulating film is formed in a corner portion of the second concave portion. Fig. 11 depicts an illustrative implementation of the claim 4 invention where an insulating film is formed on the second conductive film, and the second concave portion is filled with the insulating film, the second gate insulating film and the second conductive film. Also, Fig. 11 shows an illustrative implementation of the claim 5 invention where the second concave portion is filled with the second gate insulating film and the second conductive film, and a surface of the second conductive film is substantially flat.

Fig. 6 depicts an illustrative implementation of the claim 6 invention where the semiconductor substrate is an SOI substrate. Fig. 15 shows an illustrative implementation of the claim 7 invention where the semiconductor device additionally includes an element isolating

region formed within the first concave portion such that the second gate insulating film and the second conductive film are allowed to extend over the element isolating region; a contact electrically connected to a portion of the second conductive film which is positioned on the element isolating region; and a wiring electrically connected to the contact.

Fig. 16 depicts an illustrative implementation of the claim 8 invention where a plurality of second concave portions are formed in the semiconductor substrate such that the second concave portions are filled with the second gate insulating film and the second conductive film, and a surface of the second conductive film is substantially flat. Fig. 17 shows an illustrative implementation of the claim 9 invention where a plurality of gate electrodes each consisting of the second conductive film is formed in the second concave portion.

Figs. 18-21 depict illustrative implementations of the claim 10 invention where an impurity concentration in the second conductive film is higher than an impurity concentration in the semiconductor substrate. The second insulating film can function as insulating film for an anti-fuse portion as described in the first, second, third and fourth embodiments described in the specification or a capacitor element as described in the fifth embodiment. *See e.g.*, Specification, p. 35, ll. 8-12.

ISSUES

Whether claims 1-11 are patentable pursuant to 35 U.S.C. § 103(a) over the combination of Chen, Bracchitta, and Wolf.

GROUPING OF CLAIMS

In accordance with 37 C.F.R. § 1.192(c)(7), Appellants respectfully assert that claims 1-11 stand or fall together.

ARGUMENT

Independent claim 1 calls for, *inter alia*, a second concave portion formed in a semiconductor substrate and having a depth from a top surface of the semiconductor substrate, substantially equal to a depth of a first concave portion.

The final office action contends that the combination of Chen, Bracchitta, and Wolf results in the invention of claim 1. To show the feature of a second concave portion as claimed, the action relies on Chen. Referring to Fig. 1 of Chen, the action contends that the depths of protection cell 10 and antifuse cell 12 are substantially equal. Appellants respectfully disagree.

The final action asserts that the protection cell 10 of Chen "has more than one portion, one of which is the same depth as the other concave portion 12, as recited, and a deeper portion." Applicants respectfully disagree with this characterization of the protection cell 10.

The crux of this appeal focuses on the definition of the claim term "concave portion" and more specifically "concave". According to the Merriam Webster online Dictionary "concave" means "arched in : curving in -- used of the side of a curve or surface on which neighboring normals to the curve or surface converge and on which lies the chord joining two neighboring points of the curve or surface".[1] In this regard, appellants submit that a concave portion must have physical boundaries defined by walls. Applying this definition, it becomes clear that Chen does not teach or suggest a second concave portion formed in a semiconductor substrate and

[1] http://www.m-w.com/cgi-bin/dictionary?book=Dictionary&va=concave

having a depth from a top surface of the semiconductor substrate, substantially equal to a depth of a first concave portion as recited in claim 1.

Chen discloses forming a stepped section at the bottom surface of the protection cell 10. Namely, the bottom surface of the protection cell 10 includes a flat portion with a constant depth X from the top surface and a slanted portion with an increasing depth from the top surface between Y and a value less than X. Appellants acknowledge that the depth X of the protection cell from a top surface to the flat portion of the bottom surface is the same as the depth X of the antifuse cell 12. Appellants further acknowledge that antifuse cell 12 is a concave portion.

Nonetheless, the flat portion of the bottom surface of the protection cell 10 does not constitute a concave portion because there is not a physical boundary in the form of a concave wall encompassing only the flat portion of the bottom surface. The protection cell has two concave portions, one portion including the entire bottom surface of the protection cell which is encompassed by the physical walls of the protection cell 10 and a second portion within the first portion, defined by an interior wall formed from the corner 20 to the bottom surface of the slanted portion at the depth Y and the exterior wall of the protection cell 10 as shown in Fig 2. Notably, the second concave portion has a variable depth, and further does not even extend to a top surface of the semiconductor substrate. The first concave portion of the protection cell 10 constitutes nothing more than a concave portion with variable depths of X to Y from the top surface to the bottom surface. Therefore, the protection cell 10 does not have a depth from a top surface of the semiconductor substrate, substantially equal to a depth of the antifuse cell 12. In sum, Chen neither teaches nor suggests a second concave portion formed in the semiconductor substrate and having a depth from a top surface of the semiconductor substrate, substantially

equal to a depth of the first concave portion as called for in claim 1. Neither Bracchitta nor Wolf remedies the defects of Chen. Thus, the combination of the applied art, even if proper, does not result in the claim 1 invention.

CONCLUSION

For all of the foregoing reasons, Appellants respectfully submit that the final rejection of claims 1-11 is improper and should be reversed.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: December 11, 2003 By: 

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APPENDIX

CLAIMS INVOLVED IN THE APPEAL

1. A semiconductor device, comprising:

a first concave portion for element isolation, formed in a semiconductor substrate;

a second concave portion formed in the semiconductor substrate and having a depth from a top surface of the semiconductor substrate, substantially equal to a depth of the first concave portion;

a first gate insulating film formed on a selected portion of said semiconductor substrate;

a second gate insulating film formed in at least a bottom surface of said second concave portion;

a first conductive film formed on said first gate insulating film; and

a second conductive film formed on said second gate insulating film.

2. The semiconductor device according to claim 1, wherein the second gate insulating film and the second conductive film are formed on the bottom surface of the second concave portion, on at least one side surface of the second concave portion and on the semiconductor substrate, and a top surface of the first conductive film is flush with a surface of the second conductive film formed on the semiconductor substrate.

3. The semiconductor device according to claim 1, wherein the second gate insulating film is formed in a corner portion of the second concave portion.

4. The semiconductor device according to claim 1, wherein an insulating film is formed on the second conductive film, and the second concave portion is filled with the insulating film, the second gate insulating film and the second conductive film.

5. The semiconductor device according to claim 1, wherein the second concave portion is filled with the second gate insulating film and the second conductive film, and a surface of the second conductive film is substantially flat.

6. The semiconductor device according to claim 1, wherein the semiconductor substrate is an SOI substrate.

7. The semiconductor device according to claim 1, further comprising:

an element isolating region formed within the first concave portion such that the second gate insulating film and the second conductive film are allowed to extend over said element isolating region;

a contact electrically connected to a portion of the second conductive film which is positioned on the element isolating region; and

a wiring electrically connected to said contact.

8. The semiconductor device according to claim 1, wherein a plurality of second concave portions are formed in the semiconductor substrate such that the second concave portions are filled with the second gate insulating film and the second conductive film, and a surface of the second conductive film is substantially flat.

9. The semiconductor device according to claim 1, wherein a plurality of gate electrodes each consisting of the second conductive film is formed in said second concave portion.

10. The semiconductor device according to claim 1, wherein an impurity concentration in the second conductive film is higher than an impurity concentration in the semiconductor substrate.

11. The semiconductor device according to claim 1, wherein said second insulating film functions as an insulating film for an anti-fuse portion or for a capacitor element.

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CONCLUSION

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Respectfully submitted,

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10. The semiconductor device according to claim 1, wherein an impurity concentration in the second conductive film is higher than an impurity concentration in the semiconductor substrate.

11. The semiconductor device according to claim 1, wherein said second insulating film functions as an insulating film for an anti-fuse portion or for a capacitor element.